

Amendments to the Specification:

Please replace paragraphs [0008], [0009], [0010], and [0011] with the following amended paragraphs:

[0008] According to another aspect of the invention, a circuit controls power supplied to a spindle motor and a head motor of a disk drive from a voltage source coupled to first and second voltage supply nodes, during normal operation the circuit provides a conduction path through a switching element to a motor supply node, and includes a spindle motor drive circuit and a head drive motor drive circuit that provide conduction paths from the motor supply node to the second voltage supply node to energize the spindle motor and the head motor. The circuit further includes a control circuit that operates at specified times during normal operation to cause the switching element to prevent current flow between the first voltage supply node and the motor supply node, configure the spindle motor drive circuit to cease driving the spindle motor and allow the spindle motor to supply current to the motor supply node, and configure the head motor drive circuit to energize the head motor with current flowing from ~~said~~ the first voltage supply node and current supplied by the spindle motor.

[0009] In some embodiments the circuit also includes a boost circuit coupled between ~~said~~ the first voltage supply node and ~~said~~ the motor supply node, and may further operate at the specified times during normal operation to activate the boost circuit to allow current to flow from the first voltage supply node to the motor supply node

[0010] According to another aspect of the invention, a circuit for controlling a spindle motor and a head motor of a disk drive comprises: first and second voltage supply nodes; a switching element coupled between ~~said~~ the first voltage supply node and a node, referred to as the motor supply node; a spindle motor drive circuit coupled between ~~said~~ the motor supply node and ~~said~~ the second voltage supply node, ~~said~~ the spindle motor drive circuit including nodes for coupling to respective spindle motor connection nodes; a head motor drive circuit coupled between ~~said~~ the motor supply node and ~~said~~ the second voltage supply node, ~~said~~ the head motor drive circuit including nodes for coupling to respective head motor connection nodes; a boost circuit coupled between ~~said~~ the first voltage supply node and ~~said~~ the motor supply node; and a control circuit

coupled to ~~said~~ the switching element, ~~said~~ the spindle motor drive circuit, ~~said~~ the head motor drive circuit, and ~~said~~ the boost circuit.

[0011] In this aspect, the control circuit is configured with a set of one or more spindle motor drive states wherein: ~~said~~ the switching element is set to allow current flow between said first voltage supply node and ~~said~~ the motor supply node, ~~said~~ the spindle motor drive circuit is configured to energize the spindle motor with current flowing between ~~said~~ the motor supply node and ~~said~~ the second voltage supply node, and ~~said~~ the boost circuit is not activated. The control circuit is also configured with a set of one or more regenerative braking states wherein: ~~said~~ the switching element is set to prevent current flow between ~~said~~ the first voltage supply node and ~~said~~ the motor supply node, ~~said~~ the spindle motor drive circuit is configured to allow the spindle motor to supply current to ~~said~~ the motor supply node, ~~said~~ the boost circuit is activated to allow current to flow from ~~said~~ the first voltage supply node to ~~said~~ the motor supply node, and ~~said~~ the head motor drive circuit is configured to energize the head motor with current flowing from ~~said~~ the first voltage supply node and current supplied by the spindle motor.

Please replace paragraphs [0015], [0016], [0017], and [0018] with the following amended paragraphs:

[0015] FIG. 1 is a block diagram of a ~~conventional prior art~~ system for powering and controlling a disk drive, which may be a hard disk drive (HDD);

[0016] FIG. 2 is a circuit schematic of a ~~conventional prior art~~ spindle motor and spindle motor drive circuit;

[0017] FIG. 3 is a circuit schematic of a ~~conventional prior art~~ head motor and head motor drive circuit;

[0018] FIGS. 4A and 4B are schematics showing the operation of the ~~conventional prior art~~ system during normal operation and during shutdown or power failure;

Please replace original paragraph [0025] with the following amended paragraph:

[0025] FIG. 1 is a block diagram showing relevant portions of a conventional (i.e., prior art) hard disk drive (HDD) system 10, which may be modified to incorporate one or more embodiments of the present invention. The invention is primarily concerned with controlling and powering the motors, and the figure concentrates on those aspects. As is well known, a hard disk drive mechanism includes one or more disks 15 (also referred to as platters; only one disk is shown) that are rotatably driven by a spindle motor 20. Disk 15 is coated on one or both sides with a magnetic material for storing user data and position information on a plurality of concentric tracks.

Please replace original paragraph [0033] with the following amended paragraph:

[0033] In a specific embodiment, the motor is driven in a manner that current is only ~~allowed~~ allowed to flow through two coils at a time. Thus, for a three-phase, Y-wound motor as shown, there are six possible commutation states, corresponding to the three possible pairs of coils through which current can flow, and the two possible directions of current flow. In a specific implementation, the motor has four pole pairs (eight poles), but six-pole and twelve-pole motors are also common. Since there are four pole pairs, there are four commutation cycles (or electrical cycles) per 360° mechanical rotation. The term commutation cycle or electrical cycle refers to a cycle through all the commutation states. Thus there are 24 commutation states for each 360° mechanical rotation of the spindle motor (*i.e.*, four commutation cycles where each commutation cycle spans the six commutation states).